REMARKS

Reconsideration of the above-identified patent application in view of the amendments above and the remarks following is respectfully requested.

Claims 1, 3-12, 14-31, 33-42 and 44-63 are in this case. Claims 20-30 and 50-59 were withdrawn by the Examiner from consideration as drawn to a non-elected invention. In the Office Action mailed April 20, 2006, claims 4-6, 9, 16 and 17 were rejected under § 112, second paragraph; claims 62 and 63 were rejected under § 102(e); and claims 1, 3-12, 14-19, 31, 33-42, 44-49, 60 and 61 were rejected under § 103(a). Independent claims 60-63 and dependent claims 10 and 40 now have been canceled. Independent claims 1 and 31 and dependent claims 4-9, 11, 12, 17, 18, 34-39, 41, 42 and 46-48 now have been amended.

The claims before the Examiner are directed toward a network adapter, such as a host channel adapter (HCA), and a method of its use. The network adapter includes a host interface, an outgoing packet generator, an incoming packet processor, a network output port and a network input port. The host interface couples the network interface adapter to a host processor. The network output port transmits, via a network, outgoing request packets to remote responders and outgoing response packets to remote requesters. The network input port receives, via the network, incoming response packets from remote responders and incoming request packets from remote requesters. The incoming packet processor receives and processes both incoming response packets and incoming request packets such as incoming read request packets. The outgoing packet generator generates outgoing request packets as requested by the host processor and also generates outgoing response packets in response to incoming request packets.

The outgoing packet generator includes a gather engine that gathers, from a system memory accessible via the host interface, and via a common data flow path, both write data for outgoing request packets and read data for outgoing response packets. Responsive to an incoming read request packet, the incoming packet processor prepares a read response work item in a memory location. The outgoing packet generator then reads the read response work item and generates an outgoing read response packet.

§ 112, Second Paragraph Rejections

In the Office Action mailed April 20, 2006, the Examiner rejected claims 4-6, 9, 16 and 17 under § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In general terms, the Examiner identified limitations in claims 4 ("the schedule queues"), 5 ("the queues", "the instances" (Applicant presumes that the Examiner meant "respective instances"), "the schedule queues"), 6 ("the queues", "the execution engines") and 9 ("the queues") that lack antecedent basis. The Examiner noted that this is only an exemplary listing of § 112, second paragraph rejections.

The Examiner noted that many of these rejections can be overcome by stating explicitly the membership of items in pluralities of such items. Therefore, claims 4-9, 11, 12, 17, 18, 34-39, 41, 42 and 46-48 have been amended as follows:

Claims 4-6, 8, 9, 34-36, 38 and 39: the "queues" and the "schedule queues" now are identified as belonging to the plurality of schedule queues.

Claims 5-7, 17, 18, 35, 37, 38, 47 and 48: the "transport service instances" now are identified as belonging to the plurality of transport service instances.

Claim 6: the "execution engines" have been identified with the "one or more" execution engines introduced earlier in the claim.

Claims 16 and 46: "such descriptors" have been identified with the "response descriptors" introduced earlier in the claims.

Claim 47: the "incoming read request packets" now are identified as belonging to the plurality of incoming read request packets.

Two of the Examiner's rejections under § 112, second paragraph are respectfully traversed, as follows:]

The Examiner rejected claim 16 for including the phrase "such packets" that renders the claim indefinite because it is unclear whether the packets are outgoing response packets, incoming read request packets, outgoing or incoming write packets. In fact, claim 16 explicitly recites "such outgoing response packets".

The Examiner rejected claim 17 for reciting the limitation "the plurality of the instances" that lacks antecedent basis. No such limitation is recited in claim 17.

§ 102(b) Rejections – Gasbarro et al. '004

In the Office Action mailed April 20, 2006, the Examiner rejected claims 62 and 63 under § 102(b) as being anticipated by Gasbarro et al., US Patent No. 6,948,004 (henceforth, "Gasbarro et al. '004"). The Examiner's rejection is respectfully traversed.

Claims 62 and 63 now have been canceled, thereby rendering moot the Examiner's rejection of these claims.

§ 103(a) Rejections – Pettey et al. '712 in view of Gasbarro et al. '004

In the Office Action mailed April 20, 2006, the Examiner rejected claims 1, 3-12, 14-19, 31, 33-42, 44-49, 60 and 61 under § 103(a) as being obvious over Pettey et

al., US Patent No. 6,594,712 (henceforth, "Pettey et al. '712") in view of Gasbarro et al. '004. The Examiner's rejection is respectfully traversed.

Claims 10, 40, 60 and 61 now have been canceled, thereby rendering moot the Examiner's rejection of these claims.

Pettey et al. '712 teach an InfiniBand target channel adapter (TCA) **202** of an InfiniBand I/O unit **108**. The overall structure of TCA **202** is illustrated in Figure 3. TCA **202** includes a transaction switch **302**, a bus router **306**, IB MACs **308** and PCI bus interfaces **312** and **316**. Bus router **306** performs InfiniBand transport layer operations. IB MACs **308** are the interfaces between TCA **202** and an InfiniBand fabric **114**. PCI bus interfaces **312** and **316** are the interfaces between TCA **302** and a host of TCA **302**. Transaction switch **302** directs packets, datagrams and command messages between IB MACs **308**, bus router **306** and PCI bus interfaces **312** and **316**. (Transaction switch **302** also includes packet memory blocks **304** in support of direct DRMA operations, which is the invention of Pettey et al. '712). The packets that TCA **202** can handle include the packets illustrated in Figures 10-13: SEND packets **1000**, RDMA write packets **1100**, RDMA read request packets **1200** and RDMA read response packets **1300**. It follows that the correspondences between components of the present invention, as recited in claims 1 and 31, and components of prior art TCA **302** are as in the following table:

Present invention	TCA **202**
Host interface	PCI bus interfaces **312** and **316**
Network output port	IB MAC **308**
Network input port	IB MAC **308**
Outgoing packet generator	Bus router **306**
Incoming packet processor	Bus router **306**

Figure 14 of Pettey et al. '712 is a block diagram of the logical structure of bus router **306**. Bus router **306** includes work queue management logic **1412** for processing InfiniBand work queue requests, transmit packet process logic **1414** for creating outgoing packets, receive packet process logic **1416** for processing incoming packets and completion process logic for maintaining InfiniBand completion queues. Bus router **306** also includes a work queue memory **1402** in support of work queue management logic **1412**, a TxPP scratchpad memory in support of transmit packet process logic **1414** and a RxPP scratchpad memory in support of receive packet process logic **1416**.

Pettey et al. '712 are silent concerning the internal architecture of the various logics of bus router **306**. In response to the Office Action mailed October 12, 2005, Applicant attempted to distinguish the present invention from the teachings of Pettey et al. '712 by adding to claim 1 the limitation that the outgoing packet generator includes a gather engine that gathers write data for outgoing write request packets and read data for outgoing read response packets via a common data flow path, and by adding a corresponding limitation to claim 31. In the Office Action mailed April 20, 2006, the Examiner cited Gasbarro et al. '004 as teaching these limitations. Applicant respectfully disagrees, and reserves the right to traverse this interpretation of Gasbarro et al. '004 later in the prosecution of the above-identified patent application. For now, to expedite the prosecution, Applicant has chosen to distinguish the present invention from the prior art cited by the Examiner by amending claims 1 and 31 to include the limitations of claims 10 and 40, respectively. Correspondingly, claims 10 and 40 have been canceled.

Specifically, the limitation of claims 10 and 40 that distinguishes the present invention from the prior art cited by the Examiner is that the incoming packet

processor prepares a read response work item, in a memory location, that is read by the outgoing packet generator to tell the outgoing packet generator how to generate the corresponding read response packet. In the embodiment of the present invention that is described in the specification, this read response work item is the "quasi-WQE" that is prepared by TCU 52 in RDB 40 in response to the receipt of a RDMA read request from a remote requester, as described in the specification on page 19 line 27 through page 20 line 7. As described in the specification on page 20 lines 8-19, execution unit 60 and SDE 66 treat quasi-WQEs the same as WQEs received from host 24. It is this emulation of the standard InfiniBand WQE mechanism by the network adapter (HCA 22 in the embodiment described in the specification) for remote requester RDMA read requests, independently of the host of the network interface adapter, that enables the present invention to use the same gather engine (SDE 66 in the embodiment described in the specification) to gather data for both requester and responder outgoing packets via the same data flow path.

By contrast, the prior art cited by the Examiner uses the standard InfiniBand WQE mechanism, in which WQEs are generated by the host, to specify data to be sent to a remote requester in response to a RDMA read request. For example, Pettey et al. '714 illustrate in Figure 18a their direct RDMA write in response to the receipt of a SEND packet as illustrated in Figure 15. The location in local memory **218** of the data to be sent to the requester is specified in step **1808** of Figure 18 by a WQE generated by host CPU **208**, as described in column 17 lines 21-22:

> Next the CPU **208** creates a DRDMA Write WQE **800** of FIG. 8 and submits it to the TCA **202**, in step **1808**.

There is neither a hint nor a suggestion in the prior art cited by the Examiner of a channel adapter such as TCA **202** of Pettey et al. '714 generating its own WQE

equivalents, independently of its host, in response to packets received from remote requesters.

With independent claims 1 and 31 allowable in their present form it follows that claims 3-9, 11, 12, 14-19, 31, 33-39, 41, 42 and 44-49 that depend therefrom also are allowable.

Other Amendments to the Claims

In responding to the Office Action mailed October 12, 2005, Applicant inadvertently neglected to amend claim 34 to depend from claim 31 instead of from claim 32. This oversight now has been corrected.

In view of the above amendments and remarks it is respectfully submitted that independent claims 1 and 31, and hence dependent claims 3-9, 11, 12, 14-19, 31, 33-39, 41, 42 and 44-49 are in condition for allowance. Prompt notice of allowance is respectfully and earnestly solicited.

Respectfully submitted,

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Date: October 18, 2006